WHAT IS CLAIMED IS:

1. An integrated circuit comprising:

a first on-chip impedance termination circuit coupled to a first pad of the integrated circuit;

a second on-chip impedance termination circuit coupled to a second pad of the integrated circuit;

a first control circuit that adjusts the impedance of the first on-chip impedance termination circuit; and

a second control circuit that adjusts the impedance of the second on-chip impedance termination circuit independently of the impedance of the first on-chip impedance termination circuit.

2. The integrated circuit according to claim 1 further comprising:

a third on-chip impedance termination circuit coupled to a third pad of the integrated circuit; and

a third control circuit that adjusts the impedance of the third on-chip impedance termination circuit independently of the first and the second impedance termination circuits.

3. An integrated circuit comprising:

a first on-chip impedance termination circuit coupled to a first pad of the integrated circuit;

a second on-chip impedance termination circuit coupled to a second pad of the integrated circuit;

a first control circuit that receives a first signal indicative of an off-chip resistance and a second signal that indicates an adjusted impedance value for the first pad, the first control circuit adjusting the impedance of the first on-chip impedance termination circuit to a first impedance value in response to the first and the second signals; and

a second control circuit that receives the first signal and a third signal that indicates an adjusted impedance value for the second pad, the second control circuit adjusting the impedance of the second on-chip impedance termination circuit to a second impedance value in response to the first and the third signals.

4. The integrated circuit as defined in claim 3 further comprising:

a third on-chip impedance termination circuit coupled to a third pad of the integrated circuit; and

a third control circuit that receives the first signal and a fourth signal that indicates an adjusted impedance value for the third pad, the third control circuit adjusting the impedance of the third on-chip impedance termination circuit to a third impedance value in response to the first and the fourth signals.

5. An integrated circuit comprising:

a digital encoder circuit coupled to receive an analog signal indicative of an impedance of an off-chip resistor, the digital encoder circuit generating a plurality of digital signals;

a first bit shifter circuit comprising first multiplexers that receive the digital signals, wherein the first multiplexers shift the digital signals to the left in response to a first bit shift signal and to the right in response to a second bit shift signal; and

a first impedance termination circuit comprising first transistors coupled in parallel and that are each coupled to receive an output signal of one of the first multiplexers, each of the first transistors being coupled to a first pin of the integrated circuit.

6. The integrated circuit as defined in claim 5 further comprising:

a second bit shifter circuit comprising second multiplexers that receive the digital signals, wherein the second multiplexers shift the digital signals to the left in response to a third bit shift signal and to the right in response to a fourth bit shift signal; and

a second impedance termination circuit comprising second transistors coupled in parallel and that are each coupled to receive an output signal one of the second multiplexers, each of the second transistors being coupled to a second pin on the integrated circuit.

7. The integrated circuit as defined in claim 6 further comprising:

a third bit shifter circuit comprising third multiplexers that receive the digital signals, wherein the third multiplexers shift the digital signals to the left in response to a fifth bit shift signal and to the right in response to a sixth bit shift signal; and

a third impedance termination circuit comprising third transistors coupled in parallel and that are each coupled to receive an output signal one of the third multiplexers, each of the third transistors being coupled to a third pin on the integrated circuit.

8. The integrated circuit as defined in claim 5 wherein an impedance of the first impedance termination circuit decreases by about 1/2 in response to the first bit shift signal, and the impedance of the first impedance termination circuit increases by about 2 in response to the second bit shift signal.

9. The integrated circuit as defined in claim 5 wherein the first impedance termination circuit includes five transistors coupled in parallel, the digital encoder circuit generates five digital signals, and the first multiplexers include five multiplexers.

10. The integrated circuit as defined in claim 5 wherein the first multiplexers receive n digital signals from the digital encoder circuit and pass each of the n digital signals from the digital encoder circuit to the first transistors without bit shifting the n digital signals in response to a bypass signal.

11. The integrated circuit as defined in claim 5 further comprising:

a second on-chip transistor coupled to the off-chip resistor; and

an analog-to-digital converter coupled to the first transistor and generating the analog signal.

12. The integrated circuit as defined in claim 5 wherein the first multiplexers shift the digital signals to the left by two bits in response to a third bit shift signal and to the right by two bits in response to a fourth bit shift signal.

13. The integrated circuit as defined in claim 5 further comprising:

logic array blocks, each including a plurality of logic elements that are configurable to implement logic functions; and

a programmable interconnect structure connecting the logic array blocks.

14. The integrated circuit as defined in claim 5 wherein the first impedance termination circuit is coupled to provide parallel termination impedance to the first pin.

15. The integrated circuit as defined in claim 5 wherein the first impedance termination circuit is coupled to provide series termination impedance to the first pin.

16. A method for providing termination impedance to a pin on an integrated circuit, the method comprising

generating digital signals in response to a signal indicative of an impedance of an off-chip resistor;

shifting the digital signals by at least one bit to generate bit shifted signals; and

setting a total impedance of first transistors using the bit shifted signals, the first transistors being coupled in parallel and to a first pin on the integrated circuit, each of the first transistors being coupled to receive one of the bit shifted signals.

17. The method according to claim 16 wherein shifting the digital signals by at least one bit to generate the bit shifted signals further comprises shifting the digital signals to the right by one bit to increase the total impedance of the first transistors.

18. The method according to claim 16 wherein shifting the digital signals by at least one bit to generate the bit shifted signals further comprises shifting the digital signals to the left by one bit to decrease the total impedance of the first transistors.

19. The method according to claim 16 further comprising:

shifting the digital signals by at least one bit to generate second bit shifted signals; and

setting a total impedance of second transistors using the second bit shifted signals, the second transistors being coupled in parallel, each of the second transistors being coupled to a second pin on the integrated circuit and to one of the second bit shifted signals.

20. The method according to claim 19 wherein shifting the digital signals by at least one bit to generate the second bit shifted signals further comprises shifting the digital signals to the left by one bit to decrease the total impedance of the second transistors.

21. The method according to claim 16 wherein shifting the digital signals by at least one bit to generate bit shifted signals further comprises:

shifting the digital signals by two bits to generate the bit shifted signals.

22. The method according to claim 16 further comprising:

passing all of the digital signals through multiplexers to generate bypass signals; and

setting the total impedance of the first transistors using the bypass signals.

23. The method according to claim 19 wherein the first transistors are coupled to provide parallel termination impedance to the first pin; and the second transistors are coupled to provide series termination impedance to the second pin.

24. The method according to claim 16 further comprising:

generating the signal indicative of the impedance of the off-chip resistor using an analog-to-digital converter circuit coupled to the off-chip resistors and an on-chip transistor.